SUB-MICRO-GRAVITY CAPACITIVE SOI MICROACCELEROMETERS

B. Vakili Amini, R. Abdolvand, and F. Ayazi
Integrated MEMS laboratory
Georgia Institute of Technology, Atlanta, GA 30332-0250
Email: vakilia@ece.gatech.edu Tel: (404) 385-6693 Fax: (404) 385-6650

ABSTRACT

The implementation and preliminary characterization of a new in-plane capacitive microaccelerometer with sub-micro-gravity resolution (<200ng/√Hz) and very high sensitivity (15pF/g) is presented. The accelerometers are fabricated in thick (100 m) silicon-on-insulator (SOI) substrates using a 2-mask fully-dry-release process that provides large seismic mass (10milli-g), reduced capacitive gaps, and reduced in-plane stiffness. The fabricated devices were interfaced to a high resolution switched-capacitor CMOS IC that eliminates the need for area-consuming reference capacitors. The measured sensitivity is 83mV/mg (17pF/g) and the output noise floor is -91dBm/Hz at 10Hz (corresponding to an acceleration resolution of 170ng/√Hz). The IC consumes 6mW power and measures 0.65mm^2 core area.

Keywords: MEMS, Capacitive SOI Accelerometers, CMOS Interface IC, Nano-Gravity Measurement

INTRODUCTION

Sub-micro-gravity accelerometers are used for measurement of very small vibratory disturbances on platforms installed on earth, space shuttles, and space stations as well as geophysical sensing and earthquake detection. However, the available systems are bulky, complex and expensive, and consume a lot of power [1].

We had previously presented 40 m thick SOI accelerometers with 20 g/√Hz resolution and sensitivity in the order of 0.2pF/g [2]. In this work, through innovation in process and IC design, the resolution and sensitivity of the dry-released SOI accelerometers were each improved by 100× to achieve, for the first time, deep sub-micro-g resolution in a small footprint (<0.5cm^2). The figure-of-merit, defined as the ratio of the device sensitivity to its mechanical noise floor, is improved by increasing the solid seismic mass through saving some part of the handle layer attached to the proof mass (as shown in Fig. 1). Also, capacitive gap sizes are reduced through deposition of a layer of doped LPCVD poly silicon, which relaxes the trench etching process and allows for higher aspect ratios. Moreover, the sense capacitance is split into four identical sub-capacitances in a fully symmetric and differential manner (two increasing and two decreasing). Hence, the reference capacitor is absorbed in the sense capacitance of the accelerometer without compromising the sensitivity of the device or increasing area (Fig. 1). The proof mass is tied to a constant voltage source at all times and is never switched. By eliminating the need for reference capacitors, the interface architecture results in a generic front-end with significant reduction in the electronic die size. The front-end IC is implemented in the 2.5V 0.25 m 2P5M N-well CMOS process from National Semiconductor. Correlated double sampling scheme (CDS) is used for strong suppression of the low-frequency flicker noise and offset.

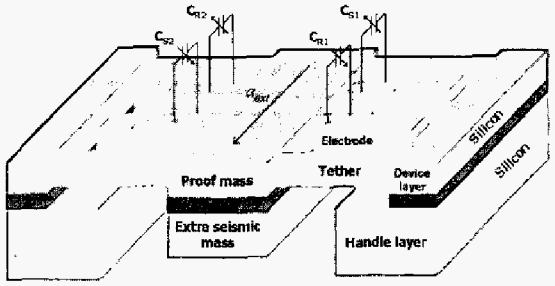

Fig 1. Schematic diagram of the fully differential capacitive SOI accelerometer with extra seismic mass

OPERATING MECHANISM AND DESIGN

Sensor target specifications are listed in Table 1. The accelerometers have been designed to achieve the goal objectives for open loop operation in air.

Table 1. Target sensor requirements

Static sensitivity	15pF/g
Brownian noise floor	<200ng/√Hz
Dynamic range	100dB
Frequency range	<200Hz
uality factor	<1
SOI thickness	100 m
Proof mass size	5mm×7mm
Overall sensor size	7mm×7mm
Mass	10milligram

The Brownian noise equivalent acceleration is expressed as

$$BNEA = \frac{\sqrt{4k_BTD}}{M} = \sqrt{\frac{4k_BT\omega_0}{MQ}} \propto \frac{1}{(capacitive\ gap)^{3/2}} \quad (1)$$

where is the Boltzmann constant, is the absolute temperature, ω is the accelerometer s natural angular frequency (first flexural mode), and is the mechanical quality factor. Increasing the mass and reducing the air damping improves this mechanical noise floor. However, reducing the damping increases the possibility of resonance (high-) and sensitivity to higher order modes, which is not desirable. Another limiting factor is the circuit noise equivalent acceleration C that depends on the

capacitive resolution of the interface IC (ΔC_{MIN}) and the capacitive sensitivity of the accelerometer (S):

$$CNEA = \frac{\Delta C_{MIN}}{S} \quad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \qquad (2)$$

The design objective is to minimize the Brownian noise equivalent acceleration ($BNEA$) and to maximize the static sensitivity (S) while satisfying process simplicity and size limitations. The proposed fabrication process enables increase of the seismic mass (to suppress the $BNEA$) and reduction of gap sizes (to increase S and reduce Q), independently. $BNEA$ is a function of capacitive gap size and reduces for larger gaps (Equation 1). Deposited polysilicon changes the tethers' thickness as well, which causes the mechanical compliance and therefore the sensitivity to start increasing for thinner poly layers. As demonstrated in Fig. 2 and Fig. 3, a capacitive gap size in between 4 to 8μm satisfies the $BNEA$ and S requirements for the target accelerometer. However, the Q should be examined to guarantee the accelerometers are in over-damped region (Fig. 4). Since the seismic mass is really large (10's of milligram) and the accelerometer is very compliant, the device is vulnerable to damage caused by mechanical shock. Hence, proper shock stops and deflection limiters should be devised to protect the accelerometer and avoid non-linear effects caused by momentum of the off-plane center of mass. ANSYS® simulation predicts the first mode shape (in-plane flexural) to occur at 180Hz and the next mode shape (out-of-plane motion) to occur at 1300Hz, which is well above the in-plane motion.

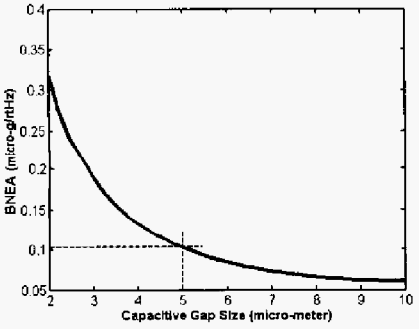

Fig. 2. $BNEA$ versus capacitive gap

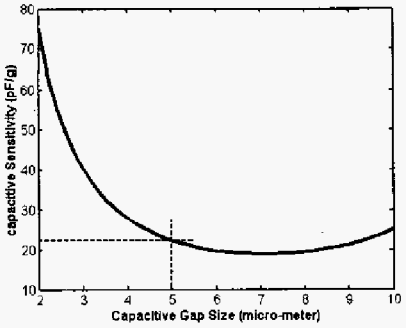

Fig. 3. Static sensitivity versus capacitive gap size

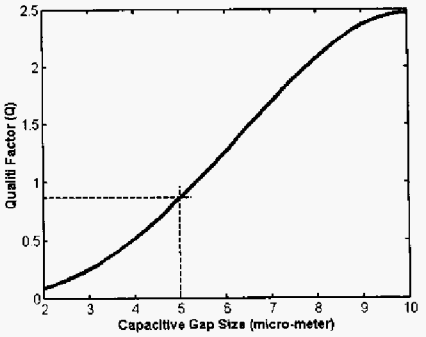

Fig. 4. Quality factor versus capacitive gap size

ACCELEROMETER FABRICATION

Figure 5 illustrates the *2-mask* fabrication process flow. It begins with growing a thick thermal silicon oxide on a low resistivity thick SOI wafer. The oxide layer is patterned on the both sides of the wafer to form the DRIE mask (Fig. 5.a). This will prevent further lithography step after the device layer is etched to define the accelerometer structure. Trenches are etched on the front side. A layer of LPCVD polysilicon is deposited and doped uniformly to reduce the capacitive gap size (Fig. 5.b). A blanket etch step removes the polysilicon at the bottom of trenches and provides isolation between bonding pads and fingers. The handle layer is then etched down to the buffer oxide (BOX) from backside. A portion of handle layer on the backside of the accelerometer proof mass will remain intact to add substantial amount of mass.

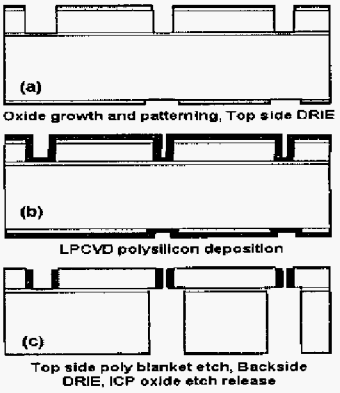

Fig. 5. Fabrication process flow

At the end, the BOX is dry etched in an ICP and the device is released (Fig. 5.c). This fully-dry process is key to the high-yield fabrication of extremely compliant structures with small gaps without experiencing stiction problems. The SEM picture of a 7mm×7mm microaccelerometer in 120μm thick SOI substrate is shown in Fig. 6. The backside of this device, showing extra seismic mass, is illustrated in Fig. 7. The proof mass is solid with no perforation that maximizes the sensitivity and minimizes the mechanical noise floor per unit area.

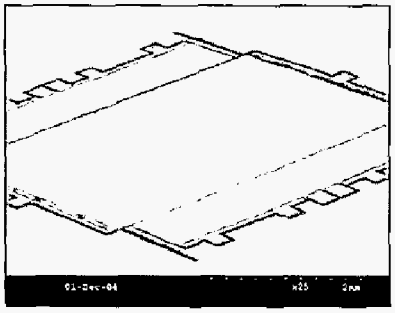

Fig. 6. SEM picture of the accelerometer from top side

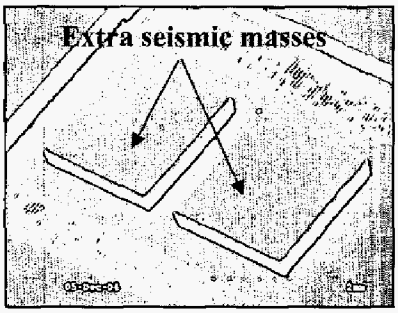

Fig. 7. SEM picture of the backside with extra masses

A close up view of the tether and sense electrodes is provided in Fig. 8. While the mask opening size between readout fingers is 9 μm, the gap has been reduced to 5μm by deposition of 2μm polysilicon on the sidewalls (Fig. 9).

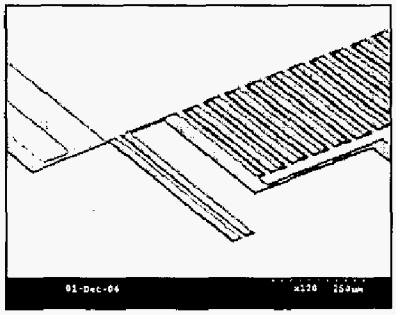

Fig. 8. Close-up of the tether and electrodes (top view) showing no residual stress

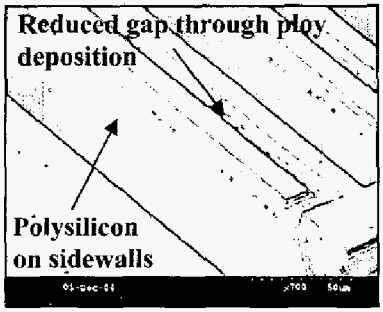

Fig. 9. Gap size reduction by polysilicon deposition

INTERFACE CIRCUIT AND TEST RESULTS

The schematic diagram of the accelerometer interface IC is shown in Fig. 10. The proposed switched-capacitor (SC) charge amplifier eliminates the need for reference capacitors and has virtually zero input offset voltage [3]. Previously reported SC charge amplifiers for capacitive sensors required on-chip reference capacitors to set the input common mode voltage [4-6]. In this architecture, the reference capacitor is absorbed in the sense capacitance of the accelerometer without compromising the sensitivity of the device or increasing area.

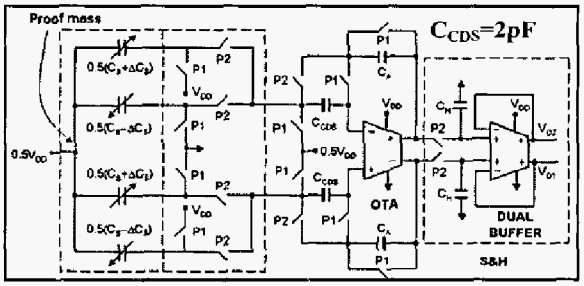

Fig. 10. Schematic diagram of the interface circuit

The interface IC was fabricated in a 0.25μm CMOS process operating from a single 2.5V supply and was wire-bonded to the accelerometer chip. A low power consumption of 6mW has been achieved. The effective die area is about 0.65mm^2. In order to reduce the *CNEA* and improve the dynamic range, low frequency noise and offset reduction techniques, i.e., correlated double sampling (CDS) and optimized transistor sizing were deployed. Moreover, the fully differential input-output scheme would reduce the background common mode noise signals. The measured sensitivity is 83mV/mg and the interface IC output noise floor is -91dBm/Hz at 10Hz, corresponding to an acceleration resolution of 170ng/√Hz (Fig. 11).

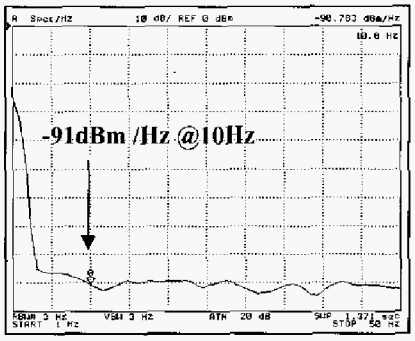

Fig. 11. IC output noise spectrum

Dynamic response of the accelerometer to an external acceleration of 16mg (peak) in a 0.46Hz bandwidth is shown in Fig.12. Due to extremely high sensitivity of the accelerometer, the device picks up any external vibration of the test setup (and hence the noisy response of Fig. 12).

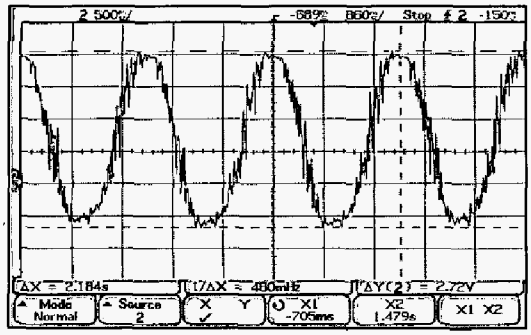

Fig. 12. Accelerometer's response to a 16mg (peak) 460mHz acceleration

The static response of the accelerometer is provided in Fig. 13. The IC output saturates with less than 30mg (<2° from earth surface). The measured specifications are summarized in Table 2.

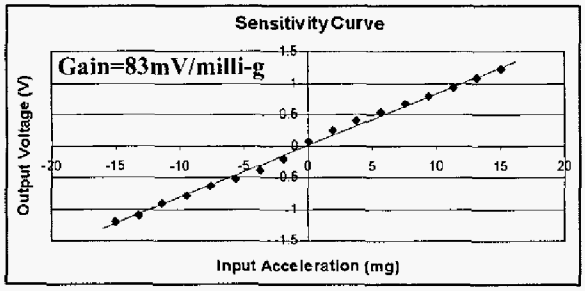

Fig. 13. Static response of the accelerometer; Measured sensitivity is 83mV/milli-g (=17pF/g)

CONCLUSION

The implementation and characterization of a novel in-plane capacitive microaccelerometer with sub-micro-gravity resolution and high sensitivity was presented. The process flow is stictionless and very simple compared to some other microaccelerometer fabrication technologies that use regular silicon substrates with multi-mask sets [7] [8]. It is a fully-dry-release process and provides the maximum sensitivity and minimum mechanical noise floor per unit area. The accelerometers were interfaced with a generic sampled data front-end IC that has the versatility of interfacing capacitive microaccelerometers with different rest capacitors. Proper mechanical design keeps the accelerometers in over-damped region in air that avoids unpredicted resonant response in the accelerometers. The measured sensitivity is 83mV/mg (17pF/g). The IC measures power consumption of 6mW and core area of 0.65mm^2.

ACKNOWLEDGEMENTS

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Table 2. MEMS + Interface circuit specifications

Accelerometer	
Dimensions: Top-side proof mass Extra seismic mass	 7mmx5mmx120μm 5mmx3mmx400μm
Proof mass	24milli-gram
Sensitivity	17pF/g
Brownian noise floor	100nano-g/√Hz
f_{-3dB} (1st-flexural)	180Hz
2nd-mode (out-of-plane)	1300Hz
Gap size	5μm
Interface IC	
Gain	83mV/milli-g
Output noise floor	-91dBm @10Hz
Min. detectable Accl.	170nano-g @10Hz
Capacitive resolution	2aF/√Hz @10Hz
Power supply	GND-2.5V
Power dissipation	6mW
Sampling frequency	200kHz
Die core area	0.65mm^2

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